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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,512	02/17/2004	Tai-Chun Huang	TS03-461	1383

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HAYNES AND BOONE, LLP
901 MAIN STREET, SUITE 3100
DALLAS, TX 75202

EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,512	HUANG ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 25* is/are pending in the application.

4a) Of the above claim(s) *9 - 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 8 and 16 - 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Election/Restrictions

2. Applicant arguments for the claims 4 and 24 are persuasive, thus, claims 4 and 24 are rejoined in this Office action as part of the Species IV (Fig. 8B).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 16, 18 and 21 – 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Kazuyasu (JP 06-244,405).

Regarding claim 16, Kazuyasu discloses in e.g., Fig. 1 and section 0002, lines 1 – 8 a semiconductor device (the device in e.g., Fig. 1; section 0001, line 1) comprising:

- semiconductor device structures (3, section 0002, line 5) formed in and on a substrate (2; see e.g., Fig. 1(b)); and

- a seal ring (4; section 0002, line 6) enclosing said semiconductor device structures forming a single die (see e.g., Fig. 1(b)),
- wherein a first distance (the distance between the corner of the element 3 to the corner of the guard ring 4) between said semiconductor device structures and a corner portion of said seal ring is smaller than a second distance (the distance between the edge of the element 3 to the side of the guard ring 4) between said semiconductor device structures and an edge portion of said seal ring (see e.g., Fig. 1(a)).

Regarding claim 18, Kazuyasu discloses in e.g., Fig. 1 said semiconductor device structures including all active devices of said semiconductor device (section 0001, line 1) except for devices used for temperature testing (Since Kazuyasu does not teach any temperature testing devices, hence Kazuyasu fully anticipates this limitation as well).

Regarding claim 21, Kazuyasu discloses in e.g., Fig. 1 said corner portion (the corner portion of the ring 4) of said seal ring (4) having a first width and wherein said edge portion (the edge portion of the ring 4) of said seal ring having a second width wherein said first width is wider than said second width (see e.g., Fig. 1(a)).

Regarding claim 22, Kazuyasu discloses in e.g., Fig. 1 said first width being "about" 1.5 times said second width or greater (see e.g., Fig. 1(a) and section 0007, lines 6 and 7).

Regarding claim 23, Kazuyasu discloses in e.g., Fig. 1 only a portion of said corner portion of said seal ring having a width wider than said second width (see e.g., Fig. 1(a)).

Regarding claim 24, Kazuyasu discloses in e.g., Fig. 1 the whole of said corner portion of the seal ring having a width wider than said second width (see e.g., Fig. 1(a)).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1 – 4, 6 – 8, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyasu in view of Towle et al. (U. S. Pat. No. 6,806,168).

Regarding claim 1, Kazuyasu discloses in e.g., Fig. 1 and section 0002, lines 1 – 8 a seal ring structure (4; section 0002, line 6) comprising:

- a substrate (2);
- a plurality of lines (4, inner and outer; e.g., Fig. 1(a)) formed overlying said substrate; and
    - wherein said plurality of lines (4, at the right, left, top and bottom) forms a continuous seal ring (see e.g., Fig. 1(a)) around a die (2; column 2, line 51) and
    - wherein a first width (the width at the corner of the chip) of said metal lines at a corner of said die is wider (see e.g., Fig. 1(a)) than a second width (the width at the side of the chip) of said lines at edges of said die (see e.g., Fig. 1(a)).

While Kazuyasu teaches a plurality of lines on top layer of the substrate, Kazuyasu does not appear to provide a plurality of layers of metal lines, a plurality of metal vias and the material of the seal ring being a metal. Towle et al. teaches in e.g., Fig. 2 a plurality of layers of metal lines (16.1; column 2, lines 29 – 32) formed overlying a substrate (18) and a plurality of metal vias (16.2; column 2, lines 32 – 33) through intermetal dielectric layers (20; column 2, lines 18 –

19) between the layers of metal lines (see e.g., Fig. 2), wherein said metal vias (16.2) interconnect said metal lines (see e.g., Fig. 2) and wherein said plurality of layers of interconnected metal lines forms a continuous seal ring (16 in Fig. 1 and column 2, lines 9 – 12) around a die (10; column 2, line 2) and the material of the lines being a metal (column 2, lines 29 – 30). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the plurality of layers of metal lines, the metal vias and the metal as the specific material of Towle et al. to form the seal ring of Kazuyasu as taught by Towle et al. to prevent the micro-cracks from propagating into the central region or active area of the die (column 2, lines 53 – 55).

Regarding claim 2, Kazuyasu, as modified, discloses said metal lines (4) being parallel to said edges (the edge of the die) of said die and wherein said metal lines are sloped at said corner of said die so that said metal lines do not have a "sharp" corner (see e.g., Fig. 1(a)).

Regarding claim 3, Kazuyasu, as modified, discloses only a portion of said corner having a width wider than said second width (see e.g., Fig. 1(a)).

Regarding claim 4, Kazuyasu, as modified, discloses in e.g., Fig. 1 the whole of said corner portion of the seal ring having a width wider than said second width (see e.g., Fig. 1(a)).

Regarding claim 6, Kazuyasu, as modified, discloses said first width being "about" 1.5 times said second width or greater (see e.g., Fig. 1(a) and section 0007, lines 6 and 7).

Regarding claim 7, Kazuyasu, as modified, discloses semiconductor device structures within said die (the die) wherein a first distance between said semiconductor device structures (3) and a corner portion of said seal ring (4) is smaller than a second distance between said semiconductor device structures (3) and an edge portion of said seal ring (4; see e.g., Fig. 1(a)).

Regarding claim 8, Kazuyasu, as modified, discloses all active semiconductor device structures (3) in said die being located within said seal ring (4) and wherein devices involved in temperature testing (i.e., thermometers or heat sensors in the wafer assembly process in a semiconductor factory) may be located outside of said seal ring (Since applicant does not specifically claim that the "devices involved in temperature testing" is for a semiconductor die, a reasonable interpretation of the term "devices involved in temperature testing" includes any thermo-devices, e.g., thermometers or heat sensors for reactors or furnace or air conditioner, etc., that locate outside of the die and inside of a factory).

Regarding claim 19, a further difference between Kazuyasu and instant invention is said seal ring (4) comprising:

- a plurality of layers of metal lines formed on said substrate; and
- a plurality of metal vias through intermetal dielectric layers between said layers of metal lines
    - o wherein said metal vias interconnect said metal lines and
    - o wherein said plurality of layers of interconnected metal lines forms a continuous seal ring around said die.

Towle et al. teaches in e.g., Fig. 2 a plurality of layers of metal lines (16.1; column 2, lines 29 – 32) formed overlying a substrate (18) and a plurality of metal vias (16.2; column 2, lines 32 – 33) through intermetal dielectric layers (20; column 2, lines 18 – 19) between the layers of metal lines (see e.g., Fig. 2), wherein said metal vias (16.2) interconnect said metal lines (see e.g., Fig. 2) and wherein said plurality of layers of interconnected metal lines forms a continuous seal ring (16 in Fig. 1 and column 2, lines 9 – 12) around a die (10; column 2, line 2)

and the material of the lines being a metal (column 2, lines 29 – 30). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the plurality of layers of metal lines, the metal vias and the metal as the specific material of Towle et al. to form the seal ring of Kazuyasu as taught by Towle et al. to prevent the micro-cracks from propagating into the central region or active area of the die (column 2, lines 53 – 55).

Regarding claim 20, Kazuyasu, as modified, discloses said interconnected metal lines being parallel to said edges of said die and wherein said interconnected metal lines are sloped at said corner of said die so that said interconnected metal lines do not have a "sharp" corner (see e.g., Fig. 1(a) of Kazuyasu).

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyasu and Towle et al. as applied to claim 1 above, and further in view of Lee (U. S. Pat. No. 5,811,874).

While Kazuyasu and Towle et al. disclose the use of the seal ring, Kazuyasu and Towle et al. do not disclose one or more slots or holes in corner of the seal ring. Lee teaches in e.g., Fig. 8 one or more slots (124; column 5, line 15) or holes (126; column 5, line 19) in corner (130; column 5, line 26) of a seal ring (112; column 5, line 14). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the one or more slots of Lee to be formed in the corner of the seal ring of Kazuyasu and Towle et al. as taught by Lee to reduce the shear stress (column 5, lines 39 – 41).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyasu in view of Cook et al. (U. S. Pat. No. 6,022,791).

While Kazuyasu discloses the use of the semiconductor device structures within the seal ring, Kazuyasu does not disclose gate electrodes, source and drain regions, and a plurality of layers of interconnected conductive lines. Cook et al. teaches in e.g., Figs. 4a, 4b and 5a gate electrodes (Gate; see e.g., Fig. 4b), source and drain regions (S/D; see e.g., Fig. 4b), and a plurality of layers of interconnected conductive lines (M0 – M6; column 4, lines 8 – 9) within a seal ring (50; column 3, lines 48 and 49). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the gate electrodes, source and drain regions, and a plurality of layers of interconnected conductive lines of Cook et al. into the structure of Kazuyasu as taught by Cook et al. to improve protection from crack penetration (column 4, lines 1 – 4).

9. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazuyasu in view of Lee (U. S. Pat. No. 5,811,874).

While Kazuyasu discloses the use of the seal ring, Kazuyasu does not disclose one or more slots or holes in corner of the seal ring. Lee teaches in e.g., Fig. 8 one or more slots (124; column 5, line 15) or holes (126; column 5, line 19) in corner (130; column 5, line 26) of a seal ring (112; column 5, line 14). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the one or more slots of Lee to be formed in the corner of the seal ring of Kazuyasu as taught by Lee to reduce the shear stress (column 5, lines 39 – 41).

Response to Arguments

10. Applicant's arguments with respect to claims 1 and 16 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Wednesday, October 04, 2006

KENNETH PARKER
SUPERVISORY PATENT EXAMINER